

1 CLAIMS:

2 1. A method of depositing polysilicon comprising:
3 positioning a substrate within a chemical vapor deposition reactor,
4 the substrate having an exposed substantially crystalline region and an
5 exposed substantially amorphous region; and

6 feeding a gaseous precursor comprising silicon to the chemical
7 vapor deposition reactor under conditions effective to substantially
8 selectively deposit polysilicon on the crystalline region and not the
9 amorphous region.

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11 2. The method of claim 1 wherein the conditions are void of
12 plasma.

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14 3. The method of claim 1 wherein the conditions include a
15 time period effective to deposit no more than about 1500 Angstroms of
16 polysilicon on the crystalline region.

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18 4. The method of claim 1 wherein the conditions include a
19 time period effective to deposit no more than about 1000 Angstroms of
20 polysilicon on the crystalline region.

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22 5. The method of claim 1 wherein the conditions comprise
23 pressure greater than 30 mTorr.

1 6. The method of claim 1 wherein the conditions comprise
2 pressure greater than 30 mTorr and temperature of less than 800°C.
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6 7. The method of claim 1 wherein the conditions are void of
7 feeding chlorine containing gas to the reactor.
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10 8. A method of depositing polysilicon comprising:
11 positioning a substrate within a hot wall low pressure chemical
12 vapor deposition reactor, the substrate having an exposed substantially
13 crystalline region, and having an exposed substantially amorphous region
14 comprising at least one of silicon dioxide and silicon nitride; and
15 feeding a gaseous silane precursor to the chemical vapor
16 deposition reactor while providing reactor temperature at from about
17 650°C to about 850°C and reactor pressure at less than or equal to
18 about 100 mTorr for a time period effective to deposit a polysilicon
19 layer substantially selectively on the crystalline region and not the
20 amorphous region to a thickness not greater than about 1500 Angstroms.
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23 9. The method of claim 8 wherein the silane comprises a
24 chlorosilane.
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27 10. The method of claim 8 wherein the reactor atmosphere
28 during the time period consists essentially of gaseous silane precursor.
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1 11. The method of claim 8 wherein the reactor atmosphere
2 during the time period is substantially void of gas comprising a
3 conductivity enhancing dopant.

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5 12. The method of claim 8 wherein the reactor atmosphere
6 during the time period comprises a gas comprising a conductivity
- enhancing dopant.

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9 13. The method of claim 8 wherein the conditions are void of
10 feeding chlorine containing gas to the reactor.

11
12 14. A method of depositing polysilicon comprising:
13 positioning a substrate within a chemical vapor deposition reactor,
14 the substrate having an exposed predominately crystalline region and an
15 exposed predominately amorphous region; and
16 feeding a gaseous precursor comprising silicon to the chemical
17 vapor deposition reactor under conditions effective to deposit polysilicon
18 on both the crystalline and amorphous regions, the deposited polysilicon
19 having a greater thickness over the crystalline region than over the
20 amorphous region.

1 15. The method of claim 14 wherein the deposited polysilicon
2 has a thickness of at least about 1500 Angstroms over the crystalline
3 region.

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5 16. The method of claim 14 wherein the conditions comprise
6 temperature of greater than or equal to about 650°C.

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8 17. The method of claim 14 wherein the conditions comprise
9 pressure less than or equal to about 100 mTorr.

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11 18. The method of claim 14 wherein the conditions comprise
12 pressure greater than 30 mTorr.

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14 19. The method of claim 14 wherein the conditions comprise
15 pressure greater than 30 mTorr and temperature of less than 800°C.

16

17 20. The method of claim 14 wherein the conditions are void of
18 feeding chlorine containing gas to the reactor.

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20 21. The method of claim 14 wherein the exposed crystalline
21 region is substantially crystalline and the exposed amorphous region is
22 substantially amorphous.

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22. A method of depositing polysilicon comprising:

positioning a substrate within a hot wall low pressure chemical vapor deposition reactor, the substrate having an exposed predominately crystalline region, and having an exposed predominately amorphous region comprising at least one of silicon dioxide and silicon nitride; and

feeding a gaseous silane precursor to the chemical vapor deposition reactor while providing reactor temperature at greater than or equal to about 650°C and reactor pressure at less than or equal to about 100 mTorr for a time period effective to deposit polysilicon on both the crystalline and amorphous regions, the deposited polysilicon having a greater thickness over the crystalline region than over the amorphous region.

23. The method of claim 22 wherein the deposited polysilicon has a thickness of at least about 1500 Angstroms over the crystalline region.

24. The method of claim 22 wherein the silane comprises a chlorosilane.

25. The method of claim 22 wherein the reactor atmosphere during the time period consists essentially of gaseous silane precursor.

1 26. The method of claim 22 wherein the exposed crystalline
2 region is substantially crystalline and the exposed amorphous region is
3 substantially amorphous.

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5 27. The method of claim 22 wherein the conditions comprise
6 pressure greater than 30 mTorr.

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8 28. The method of claim 22 wherein the conditions comprise
9 pressure greater than 30 mTorr and temperature of less than 800°C.

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11 29. The method of claim 22 wherein the conditions are void of
12 feeding chlorine containing gas to the reactor.

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14 30. A method of depositing polysilicon comprising:
15 providing a semiconductor wafer having an exposed monocrystalline
16 silicon region and an exposed substantially amorphous dielectric material
17 region; and

18 feeding a gaseous precursor comprising silicon to the chemical
19 vapor deposition reactor under conditions effective to substantially
20 selectively deposit polysilicon on the monocrystalline silicon region and
21 not the dielectric material region.

31. The method of claim 30 wherein the gaseous precursor comprising silicon comprises a silane.

32. The method of claim 30 wherein the gaseous precursor comprising silicon comprises a silane, and the reactor atmosphere during depositing consists essentially of gaseous silane precursor.

33. The method of claim 30 wherein the conditions comprise pressure greater than 30 mTorr.

34. The method of claim 30 wherein the conditions comprise pressure greater than 30 ~~at~~ Torr and temperature of less than 800°C.

35. The method of claim 30 wherein the conditions are void of feeding chlorine containing gas to the reactor.

36. The method of claim 30 wherein the conditions comprise temperature of greater than or equal to about 650°C and pressure less than or equal to about 100 mTorr, and wherein the gaseous precursor comprising silicon comprises a silane, and the reactor atmosphere during depositing consists essentially of the silane.

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2 37. A method of fabricating a field effect transistor on a
substrate comprising:

3 forming a gate dielectric layer and a gate over semiconductive
4 material;

5 forming substantially amorphous insulating material over and
6 laterally proximate the gate;

7 etching through the substantially amorphous insulating material to
8 expose semiconductive material over at least one desired source/drain
9 region laterally proximate at least one side of the gate and having the
10 gate protectively covered with substantially amorphous insulating material
11 proximate the etched portion;

12 providing the substrate after etching within a chemical vapor
13 deposition reactor; and

14 feeding a gaseous precursor comprising silicon to the chemical
15 vapor deposition reactor under conditions effective to substantially
16 selectively deposit polysilicon on the source/drain region and not on
17 substantially amorphous material, and forming an elevated source/drain
18 on the one source/drain region.

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20 38. The method of claim 37 wherein the gaseous precursor
21 comprising silicon comprises a silane.

39. The method of claim 37 wherein the gaseous precursor comprising silicon comprises a silane, and the reactor atmosphere during depositing consists essentially of gaseous silane precursor.

40. The method of claim 37 wherein the conditions comprise pressure greater than 30 mTorr.

41. The method of claim 37 wherein the conditions comprise pressure greater than 30 mTorr and temperature of less than 800°C.

42. The method of claim 37 wherein the conditions are void of feeding chlorine containing gas to the reactor.

43. The method of claim 37 wherein the conditions comprise temperature of less than 800°C and pressure greater than 30 mTorr, and wherein the gaseous precursor comprising silicon comprises a silane, and the reactor atmosphere during depositing consists essentially of the silane.

1 44. A method of fabricating a field effect transistor on a
2 substrate comprising:

3 forming a gate dielectric layer and a gate over semiconductive
4 material;

5 forming doped source/drain regions within semiconductive material
6 laterally proximate the gate;

7 forming substantially amorphous insulating material over and
8 laterally proximate the gate;

9 providing the substrate within a chemical vapor deposition reactor;
10 and

11 feeding a gaseous precursor comprising silicon to the chemical
12 vapor deposition reactor under conditions effective to substantially
13 selectively deposit polysilicon on the source/drain regions and not on
14 substantially amorphous material, and forming elevated source/drains on
15 the doped source/drain regions.

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17 45. The method of claim 44 wherein the conditions are void of
18 feeding chlorine containing gas to the reactor.

1 46. A method of forming a contact to a substrate comprising:
2 forming substantially amorphous insulating material over a substrate
3 node location;
4 etching a contact opening through the amorphous insulating
5 material over the node location;
6 providing the node location to comprise an outwardly exposed
7 substantially crystalline surface;
8 providing the substrate with outwardly exposed substantially
9 crystalline node location surface within a chemical vapor deposition
10 reactor; and
11 feeding a gaseous precursor comprising silicon to the chemical
12 vapor deposition reactor under conditions effective to substantially
13 selectively deposit polysilicon on the outwardly exposed crystalline node
14 location surface and not on the insulating material.

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16 47. The method of claim 46 wherein the crystalline surface
17 comprises a silicide.

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19 48. The method of claim 46 wherein the crystalline surface
20 comprises a silicide formed over monocrystalline silicon.

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22 49. The method of claim 46 wherein the conditions comprise
23 pressure greater than 30 mTorr.

1 50. The method of claim 46 wherein the conditions comprise
2 pressure greater than 30 mTorr and temperature of less than 800°C.
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6 51. The method of claim 46 wherein the conditions are void of
7 feeding chlorine containing gas to the reactor.
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10 52. A method of forming a contact to a substrate comprising:
11 forming substantially amorphous insulating material over a substrate
12 node location comprising crystalline silicon;
13 etching a contact opening through the amorphous insulating
14 material to the crystalline silicon of the node location;
15 providing the substrate with etched contact opening within a
16 chemical vapor deposition reactor; and
17 feeding a gaseous precursor comprising silicon to the chemical
18 vapor deposition reactor under conditions effective to substantially
19 selectively deposit polysilicon within the contact opening on the
20 crystalline silicon of the node location and not on the insulating
21 material.

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24 53. The method of claim 52 wherein the crystalline silicon is
25 monocrystalline silicon.

54. The method of claim 52 wherein the crystalline silicon is polycrystalline silicon.

55. The method of claim 52 wherein the gaseous precursor comprising silicon comprises a silane, and wherein pressure during deposition is greater than 30 mTorr.

56. The method of claim 52 wherein the conditions are void of feeding chlorine containing gas to the reactor.

57. A method of forming a capacitor comprising:
providing a substrate within a chemical vapor deposition reactor,
the substrate having an exposed substantially crystalline region and an
exposed substantially amorphous region;

feeding a gaseous precursor comprising silicon to the chemical vapor deposition reactor under conditions effective to substantially selectively deposit polysilicon on the crystalline region and not the amorphous region, and forming the polysilicon into a first capacitor electrode;

forming a capacitor dielectric layer over the polysilicon; and
forming a second capacitor electrode over the capacitor dielectric
layer.

1 58. The method of claim 57 wherein the conditions comprise
2 pressure greater than 30 mTorr and temperature of less than 800°C.

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4 59. The method of claim 57 wherein the conditions are void of
5 feeding chlorine containing gas to the reactor.

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7 60. A method of forming a capacitor comprising:
8 forming a first capacitor electrode over a substrate;
9 forming a substantially crystalline capacitor dielectric layer over the
10 first capacitor electrode;
11 providing the substrate with substantially crystalline capacitor
12 dielectric layer within a chemical vapor deposition reactor; and
13 feeding a gaseous precursor comprising silicon to the chemical
14 vapor deposition reactor under conditions effective to substantially
15 selectively deposit polysilicon on the crystalline region, and forming the
16 polysilicon into a second capacitor electrode. (43)

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18 61. The method of claim 60 wherein the conditions comprise
19 pressure greater than 30 mTorr and temperature of less than 800°C.

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21 62. The method of claim 60 wherein the conditions are void of
22 feeding chlorine containing gas to the reactor. (43)

63. The method of claim 60 wherein the crystalline capacitor dielectric layer comprises barium strontium titanate. *BST*

64. The method of claim 60 wherein the crystalline capacitor dielectric layer comprises Ta_2O_5 .

Tantalum

TaO₂

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